

## WHAT IS CLAIMED IS:

1           1. An apparatus for computing the absolute value of a  
2 complex number having a real part and an imaginary part, the  
3 apparatus comprising:  
4           a first squaring unit having an input receiving said real  
5 part of said complex number and an output generating a first  
6 square of said real part multiplied with itself;  
7           a second squaring unit having an input receiving said  
8 imaginary part of said complex number and an output generating  
9 a second of said imaginary part multiplied with itself;  
10          a summing unit having a first input receiving said first  
11 square, having a second input receiving said second square and  
12 an output generating a sum of said first square and said  
13 second square; and  
14          a square root unit having an input receiving said sum and  
15 an output generating a square root of said sum, said square  
16 root being said absolute value of said complex number.

1           2. The apparatus of claim 1, wherein the real and  
2 imaginary parts of the complex number are each represented by  
3 a digital number of B bits, where B is even and wherein:  
4           said first squaring unit and said second squaring unit  
5 each include:  
6           a first multiplier having a first input receiving a  
7 set of B least significant bits of said input, a second  
8 input receiving said set of B least significant bits of  
9 said input and a product output generating a first  
10 product of said B least significant bits multiplied by  
11 itself,

12           a second multiplier having a first input receiving a  
13       set of B most significant bits of said input, a second  
14       input receiving said set of B most significant bits of  
15       said input and a product output generating a second  
16       product of said B most significant bits multiplied by  
17       itself,

18           a third multiplier having a first input receiving  
19       said set of B least significant bits of said input, a  
20       second input receiving said set of B most significant  
21       bits of said input and a product output generating a  
22       third product of said B least significant bits multiplied  
23       by said B most significant bits,

24           a shift unit having an input receiving said product  
25       output of said third multiplier and a shift output  
26       generating a left shifted output left shifted by  $(B/2)+1$   
27       bits, and

28           a summing unit having a first input having least  
29       significant bits receiving said first product and most  
30       significant bits receiving said second product, a second  
31       input receiving said left shifted output and generating a  
32       sum output being a sum of said first and second inputs,  
33       said sum output being said output of said squaring unit.

1           3.   The apparatus of claim 2, wherein the real and  
2       imaginary parts of the complex number are each represented by  
3       a signed digital number, and wherein:

4           said first multiplier of each of said first and second  
5       squaring units is unsigned multipliers;

6        said second and third multipliers of each of said first  
7 and second squaring unit are a signed multiplier; and  
8        said summing unit is a signed summing unit.

1        4. The apparatus of claim 2, wherein:

2        B is an integral factor of 4; and

3        said first multiplier of each of said first squaring unit  
4 and said second squaring unit includes

5            a fourth multiplier having a tenth input receiving a  
6 set of B/4 least significant bits of said first input of  
7 said corresponding multiplier, a second input receiving  
8 said set of B/4 least significant bits of said first  
9 input of said corresponding multiplier and a product  
10 output generating a fourth product of said B/4 least  
11 significant bits multiplied by itself,

12            a fifth multiplier having a first input receiving a  
13 set of B/4 most significant bits of said first input of  
14 said corresponding multiplier, a second input receiving  
15 said set of B/4 most significant bits of said first input  
16 of said corresponding multiplier and a product output  
17 generating a fifth product of said B/4 most significant  
18 bits multiplied by itself,

19            a sixth multiplier having a first input receiving  
20 said set of B/4 least significant bits of said first  
21 input of said corresponding multiplier, a second input  
22 receiving said set of B/4 most significant bits of said  
23 first input of said corresponding multiplier and a  
24 product output generating a sixth product of said B/4  
25 least significant bits multiplied by said B/4 most  
26 significant bits,

27           a shift unit having an input receiving said output  
28   of said sixth multiplier and a shift output generating an  
29   left shifted output left shifted by  $(B/4)+1$  bits, and  
30           a summing unit having a first input having least  
31   significant bits receiving said third product and most  
32   significant bits receiving said fourth product, a second  
33   input receiving said left shifted output and generating a  
34   sum output being a sum of said first and second inputs,  
35   said sum output being said output of said multiplier.

1           5.   The apparatus of claim 1, wherein the real and  
2   imaginary parts of the complex number are each represented by  
3   a digital number of B bits, where B odd even and wherein:

4           said first squaring unit and said second squaring unit  
5   each include:

6           a first multiplier having a first input receiving a  
7   set of  $(B-1)/2$  least significant bits of said input, a  
8   second input receiving said set of  $(B-1)/2$  least  
9   significant bits of said input and a product output  
10   generating a first product of said  $(B-1)/2$  least  
11   significant bits multiplied by itself,

12           a second multiplier having a first input receiving a  
13   set of  $(B+1)/2$  most significant bits of said input, a  
14   second input receiving said set of  $(B+1)/2$  most  
15   significant bits of said input and a product output  
16   generating a second product of said  $(B+1)/2$  most  
17   significant bits multiplied by itself,

18           a third multiplier having a first input receiving  
19   said set of  $(B-1)/2$  least significant bits of said input,  
20   a second input receiving said set of  $(B+1)/2$  most

21 significant bits of said input and a product output  
22 generating a third product of said  $(B-1)/2$  least  
23 significant bits multiplied by said  $(B+1)/2$  most  
24 significant bits,

25 a shift unit having an input receiving said third  
26 output of said third multiplier and a shift output  
27 generating a left shifted output left shifted by  $(B+1)/2$   
28 bits, and

29 a summing unit having a first input having least  
30 significant bits receiving said first product and most  
31 significant bits receiving said second product, a second  
32 input receiving said left shifted output and generating a  
33 sum output being a sum of said first and second inputs,  
34 said sum output being said output of said squaring unit.

1 6. The apparatus of claim 5, wherein the real and  
2 imaginary parts of the complex number are each represented by  
3 a signed digital number, and wherein:

4 said first multiplier of each of said first and second  
5 squaring units is unsigned multipliers;

6 said second and third multipliers of each of said first  
7 and second squaring unit are a signed multiplier; and

8 said summing unit is a signed summing unit.

1 7. The apparatus of claim 1, wherein the real and  
2 imaginary parts of the complex number are each represented by  
3 a digital number of B bits, where B is odd and wherein:

4 said first squaring unit and said second squaring unit  
5 each include:

6 a first multiplier having a first input receiving a  
7 set of  $(B+1)/2$  least significant bits of said input, a  
8 second input receiving said set of  $(B+1)/2$  least  
9 significant bits of said input and a product output  
10 generating a first product of said  $(B+1)/2$  least  
11 significant bits multiplied by itself,

12 a second multiplier having a first input receiving a  
13 set of  $(B-1)/2$  most significant bits of said input, a  
14 second input receiving said set of  $(B-1)/2$  most  
15 significant bits of said input and a product output  
16 generating a second product of said  $(B-1)/2$  most  
17 significant bits multiplied by itself,

18 a third multiplier having a first input receiving  
19 said set of  $(B+1)/2$  least significant bits of said input,  
20 a second input receiving said set of  $(B-1)/2$  most  
21 significant bits of said input and a product output  
22 generating a third product of said  $(B+1)/2$  least  
23 significant bits multiplied by said  $(B-1)/2$  most  
24 significant bits,

25 a shift unit having an input receiving said third  
26 output of said third multiplier and a shift output  
27 generating a left shifted output left shifted by  $(B+3)/2$   
28 bits, and

29 a summing unit having a first input having least  
30 significant bits receiving said first product and most  
31 significant bits receiving said second product, a second  
32 input receiving said left shifted output and generating a  
33 sum output being a sum of said first and second inputs,  
34 said sum output being said output of said squaring unit.

1        8. The apparatus of claim 7, wherein the real and  
2 imaginary parts of the complex number are each represented by  
3 a signed digital number, and wherein:  
4        said first multiplier of each of said first and second  
5 squaring units is unsigned multipliers;  
6        said second and third multipliers of each of said first  
7 and second squaring unit are a signed multiplier; and  
8        said summing unit is a signed summing unit.

1        9. The apparatus of claim 1, wherein:  
2        said square root unit includes a plurality of processing  
3 elements equal in number to a number of bits representing said  
4 real part and said imaginary part of said complex number  
5 disposed in a cascade chain, each processing element having  
6        a current data input, said current data input of a  
7 first processing element in said chain receiving said sum  
8 output of said summing unit,  
9        a current remainder input, said current remainder  
10 input of said first processing element in said chain  
11 receiving a zero input,  
12        a current root input, said current root input of  
13 said first processing element in said chain receiving a  
14 zero input,  
15        a next data output, said next data output connected  
16 to said current data input of a next processing element  
17 in said chain,  
18        a next remainder output, said next remainder output  
19 connected to said current remainder input of a next  
20 processing element in said chain, said next remainder

21 output of a last processing element in said chain forming  
22 a remainder part of said square root,  
23 a next root output, said next root output connected  
24 to said current root input of a next processing element  
25 in said chain, said next root output of said last  
26 processing element in said chain forming an integer part  
27 of said square root,  
28 a shift unit having an input connected to said  
29 current data input and an output connected to said next  
30 data output, said shift unit left shifting said current  
31 data input two bits,  
32 a signed summing unit having a positive input  
33 receiving as least significant bits two most significant  
34 bits of said current data input and bits of said current  
35 remainder input left shifted two bits and a negative  
36 input having two least significant bits receiving the  
37 digital constant "01" and bits receiving said current  
38 root input left shifted two bits, said signed summing  
39 unit generating a difference output corresponding to a  
40 difference of said positive input minus said negative  
41 input and a sign bit indicating a sign of said  
42 difference,  
43 a first multiplexer having a first input receiving  
44 as least significant bits two most significant bits of  
45 said current data input and bits of said current  
46 remainder input left shifted two bits, a second input  
47 receiving said difference output, a control input  
48 receiving said sign bit and an output coupling a selected  
49 one of said first input and said second input dependent



50 upon said control input, said output connected to said  
51 next remainder output, and

52 a second multiplexer having a first input receiving  
53 as least significant bit a digital constant "0" and bits  
54 of said current root input left shifted one bit, a second  
55 input receiving as least significant bit a digital  
56 constant "1" and bits of said current root input left  
57 shifted one bit, a control input receiving said sign bit  
58 and an output coupling a selected one of said first input  
59 and said second input dependent upon said control input,  
60 said output connected to said next root output.

1 10. The apparatus of claim 9, wherein:

2 each processing element further having

3 a first data latch having an input receiving said  
4 shift unit output temporarily storing said next data  
5 output,

6 a second data latch having an input receiving said  
7 output of said first multiplexer temporarily storing said  
8 next remainder output, and

9 a third data latch having an input receiving said  
10 output of said second multiplexer temporarily storing  
11 said next root output.

1 11. The apparatus of claim 9, wherein:

2 said square root unit includes

3 at least one processing element disposed in a  
4 cascade chain, each processing element having

5           a current data input, said current data input  
6 of a first processing element in said chain  
7 receiving said sum output of said summing unit,  
8           a current remainder input, said current  
9 remainder input of said first processing element in  
10 said chain receiving a zero input,  
11           a current root input, said current root input  
12 of said first processing element in said chain  
13 receiving a zero input,  
14           a next data output, said next data output  
15 connected to said current data input of a next  
16 processing element in said chain,  
17           a next remainder output, said next remainder  
18 output connected to said current remainder input of  
19 a next processing element in said chain,  
20           a next root output, said next root output  
21 connected to said current root input of a next  
22 processing element in said chain,  
23           a shift unit having an input connected to said  
24 current data input and an output connected to said  
25 next data output, said shift unit left shifting  
26 said current data input two bits,  
27           a signed summing unit having a positive input  
28 receiving as least significant bits two most  
29 significant bits of said current data input and  
30 bits of said current remainder input left shifted  
31 two bits and a negative input having two least  
32 significant bits receiving the digital constant  
33 "01" and bits receiving said current root input  
34 left shifted two bits, said signed summing unit

35 generating a difference output corresponding to a  
36 difference of said positive input minus said  
37 negative input and a sign bit indicating a sign of  
38 said difference,

39 a first multiplexer having a first input  
40 receiving as least significant bits two most  
41 significant bits of said current data input and  
42 bits of said current remainder input left shifted  
43 two bits, a second input receiving said difference  
44 output, a control input receiving said sign bit and  
45 an output coupling a selected one of said first  
46 input and said second input dependent upon said  
47 control input, said output connected to said next  
48 remainder output, and

49 a second multiplexer having a first input  
50 receiving as least significant bit a digital  
51 constant "0" and bits of said current root input  
52 left shifted one bit, a second input receiving as  
53 least significant bit a digital constant "1" and  
54 bits of said current root input left shifted one  
55 bit, a control input receiving said sign bit and an  
56 output coupling a selected one of said first input  
57 and said second input dependent upon said control  
58 input, said output connected to said next root  
59 output;

60 a switch having

61 a first data input receiving said sum output  
62 of said summing unit,

63 a second data input receiving said next data  
64 output of a last processing element in said chain,

65           a remainder input receiving said next  
66 remainder output of said last processing element in  
67 said chain,  
68           a root input receiving said next root output  
69 of said last processing element in said chain,  
70           a data output connected to said current data  
71 input of a first processing element in said chain,  
72           a first remainder output connected to said  
73 current remainder input of said first processing  
74 element in said chain,  
75           a first root output connected to said current  
76 root of said first processing element in said  
77 chain,  
78           a second remainder output a remainder part of  
79 said square root, and  
80           a second root output forming an integer part  
81 of said square root,  
82           said switch having a first state connecting said  
83 first input data to said data output, a digital constant  
84 "0" to said first remainder output, a digital constant  
85 "0" to said first root output and said root input to said  
86 second root output,  
87           said switch having a second state connecting said  
88 second data input to said data output, said remainder  
89 input to said first remainder output and said root input  
90 to said first root output; and  
91           a loop control connected to said switch, said loop  
92 control controlling said first and second states of said  
93 switch to input data to said chain of processing  
94 elements, recirculate said data, remainder and root from

95        said last processing element in said chain to said first  
96        processing element in said chain at least once, and  
97        output a calculated root.

1        12. The apparatus of claim 11, wherein:  
2        said first state of said switch further connects said  
3        remainder input to said remainder output.

1        13. The apparatus of claim 11, wherein:  
2        each processing element further having  
3            a first data latch having an input receiving said  
4        shift unit output temporarily storing said next data  
5        output,  
6            a second data latch having an input receiving said  
7        output of said first multiplexer temporarily storing said  
8        next remainder output, and  
9            a third data latch having an input receiving said  
10       output of said second multiplexer temporarily storing  
11       said next root output.